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Algorithm Implementation for Power Reduction in MTCMOS Circuits

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Abstract: *Using MTCMOS for enabling high performance and low power consumption is increasing exponentially and for this optimum power gating sleep transistor design and implementation are critical. This paper describes various issues related in sizing sleep transistors like optimization in area, IR drop consideration and sleep transistor efficiency. This paper describes method for increasing the area efficiency and all the other factor that needs to be kept mind for designing sleep transistors. This paper also proposes algorithm and flowchart on how to cluster sleep transistors attach with each gate and hence increasing the efficiency.*

1. INTRODUCTION

With technology scaling the leakage power has been increasing exponentially [1] [2]. Using MTCMOS technology high performance and low power operation can be achieved by utilising high and low V_t transistors [3] [4] [5].

By using low V_t transistors in signal path, the supply voltage can be lowered in order to reduce power dissipation but reducing V_t will exponentially increase subthreshold current [6]. The most effective method for reducing exponentially increase subthreshold current [6]. The most effective method for reducing leakage is power gating. In this method sleep transistors are used to shut power supplies in standby mode. SLEEP signal (active\standby mode) is used for controlling sleep transistors. During active mode sleep transistors can be realized as resistors as shown in Fig. 1. But the implementation of sleep transistors is also challenging. If we add more sleep transistors then there is significant area penalty in the design. Moreover when the design is coming out of sleep mode and charged by sleep transistors there will be large power on current rush which will eventually cause large IR drop which in turn will cause malfunction in the design. The design cycle is kept short but at the expense of slight speed loss. No methodologies have been developed to size high V_t sleep transistors that trades off area and performance. This paper presents efficient clustering technique which focuses on reducing the area and leakage of the design. It provides algorithm in order to implement this technique.

2. APPROACH

In active mode sleep transistors can be realized as resistor R. Due to this resistance there will be voltage drop equal to IR where I is current flowing through sleep transistors. This voltage drop reduces gates driving capability from V_{dd} to V_{dd}-V_x which will degrade gates performance. Hence to improve gate performance resistor should be made small which in turn will increase the size of sleep transistor and hence there will be increase in area and power overhead. And if resistor is made large then sleep transistors will be small but speed of the gate will decrease. The worst case of design can happen if all the gates supported by sleep transistors are switched on simultaneously and in this case $I=I_1+I_2+I_3$ as shown in Fig. 2.

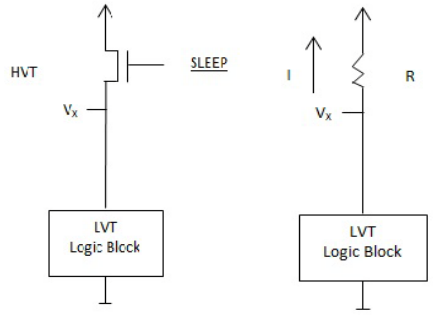

Fig. 1

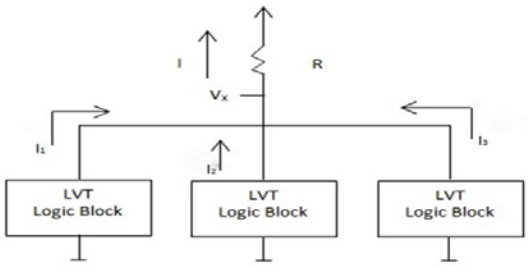

Fig. 2

But if there is mutually exclusive discharging of gates then sleep transistors are sized according to maximum current of mutually exclusive discharging gates (I=max { I_1,I_2,I_3}). Hence in this case size of the sleep transistors is smaller in this case.

3. SIZING OF THE SLEEP TRANSISTOR [7]

Delay of a single gate(τ_d) in the absence of sleep transistor can be expressed as:

$$\tau_d = \frac{C_L V_{DD}}{(V_{dd} - V_{tL})^{\alpha}}$$

Delay of a single gate(τ_d) in the presence of sleep transistor can be expressed as:

$$\tau_d^{sleep} = \frac{C_L V_{dd}}{(V_{dd} - V_x - V_{tL})^{\alpha}}$$

C_L=Load Capacitance at the gate's output
V_{tL}=350mV
V_{dd}=1.8V
α=velocity saturation index 1.3 in 0.18µm CMOS technology
V_x=potential of virtual ground
We assume that there is 5% degradation in the performance in the presence of sleep transistor, therefore:

$$\frac{\tau_d}{\tau_d^{sleep}} = 95\%$$

Substituting the value of τ_d and τ_d^{sleep} and assuming the value of α=1 for simplicity, we get

$$1 - \frac{V_x}{(V_{dd} - V_{tL})} = 95\%$$

Therefore,

$$V_x = 0.05(V_{dd} - V_{tL})$$

The current flowing through the linearly operating sleep transistor can be expressed as:

$$I_{sleep} = \mu_n C_{ox} \left(W/L\right)_{sleep} \left[(V_{dd} - V_{tH})V_x - V_{x^2}/2\right]$$

$$\approx 0.05 \mu_n C_{ox} \left(W/L\right)_{sleep} (V_{dd} - V_{tL})(V_{dd} - V_{tH})$$

μ_n=N-mobility

C_{ox}=oxide capacitance

V_{tH}=500 mV

$$\left(W/L\right)_{sleep} = \frac{I_{sleep}}{0.05 \mu_n C_{ox} (V_{dd} - V_{tH})(V_{dd} - V_{tH})}$$

I_{sleep} and $\left(W/L\right)_{sleep}$ are chosen in such a way that it exhibit low power dissipation. I_{sleep} is chosen to be 250µA leading to $\left(W/L\right)_{sleep}$ ≈6 for 0.18µm for CMOS technology. The efficiency of sleep transistor increases with increase in length of the gate and reaches peak with 130nm and it drops with increase in width of the gate till 1.6µm.

Preprocessing of gate current in order to group gates into subclusters such that the combination should not exceed the maximum current of any gate within the cluster. Random input vectors are applied and highest discharging current at the output of every gate is monitored. Then combination of this current is taken in such a way that the clustering of each should not exceed 250µA.

4. ALGORITHM AND FLOWCHART FOR THE PROCESS

1. Calculate value of current flowing across all gates.
2. Set all gates free, so that they can be clustered.
3. For all gates in the circuit
   (i) if gate **a** is not clustered then allot new cluster **X** to it and update cluster current .
   (ii) add current of gate **b** to cluster X if current value of cluster exceeds 250 then allot new cluster **Y** to the gate otherwise append that gate to cluster **X.**
4. End for
5. Return the number of clusters formed.

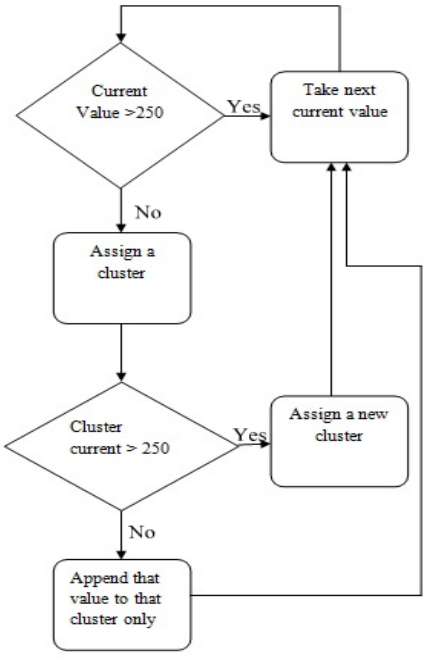

Fig. 3: Flowchart

5. RESULTS AND CONCLUSIONS

We have considered a matrix of 3x3. In this matrix we have assumed the value of current flowing through individual sleep transistors. The values are 100, 120, 70, 200, 40, 300, 70, 90,

and 20. The clustering takes place in such a way that combination of addition of these currents does not exceed 250. So in our case the no sleep transistor gets reduced from 9 to 4. This has been shown in Fig. 4.

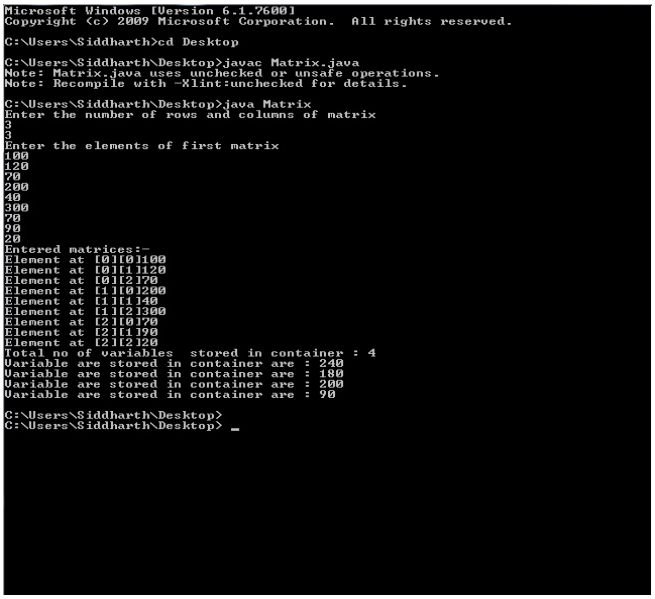

Fig. 4: Result

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